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uniquely experienced technology strategist | trans-disciplinary leader | collaborative instigator

Driven by an omnivorous curiosity and equipped with a robust foundation in applied physics, electrical engineering, and computer science, my career has been rooted in exploring the design and development of useful systems challenging conventional limits of scale & complexity. The experiences of over two decades of collaborations with highly skilled colleagues from diverse professional backgrounds has provided unparalleled opportunities to learn from and integrate perspectives across many disciplines. Along with the pragmatic focus of these unique expeditions, the process cultivated the deep exposure necessary to develop effective practices, organizational structures, communication techniques, and leadership skills in inter-disciplinary teams and cultures. From this background, I established a strong history of defining technically-grounded business strategies coupled with crafting a coherent, shared vision to motivate and guide successful delivery.

HIGHLIGHTS

Technology Strategy

Developed corporate-wide frameworks and methods for evaluating technology opportunities in conjunction with business goals and user-centered design research. Piloted and refined structured innovation programs to discover and explore new markets and business models through rapid prototyping and direct engagement of customers.

Product Design & Development

Led agile, interdisciplinary teams combining expertise and techniques of ethnography, industrial, and interaction design with world-leading technologists in board, silicon, mechanical/thermal, and software engineering to create award-winning, real-world products across a broad range of markets.

Deep expertise in evaluating approaches to highly complex and technically challenging engineering problems, particularly in the unique patterns that emerge when combining the extremes of very small parts integrated into large coordinated systems. Intensive focus on design methods and architectural approaches.

Analysis & Communication

Proven experience in synthesizing and distilling strategy to executives, communicating clear direction for internal terms, and expressing engaging value for external partners and customers.

EXPERIENCE 2008–2011

Co-Founder & Chief Technology Officer **founded November 2009**

Lux Bio Group, S.A.

Managing the technology and design strategy of a combined spin-out with a mission to leverage and expand a unique ability to bring the worlds of biotech, computing, and semiconductor manufacturing together to accelerate the revolution in digital biology.

As LBG addresses both ends of the "molecule-information" problem to close the loop in molecular analysis, this role demands a platform perspective of how sensing molecule-scale dynamics and terabyte-scale analytics relate to design a engineering-feasible and cost-effective solution that can meet immediate goals and grow to reach new opportunities over time.

Key responsibilities in making assumptions from the many different disciplines involved more explicit and their consequences more accessible when crossing from technological boundaries internally and when working with external vendors.

Director, Services Design & External Engagements **January 2008 to February 2009**

Intel, New Business Initiatives / Integrated Analytics Solutions

Integrated Analytics Solutions (IAS) focused on reducing cost & complexity in adopting data-intensive instruments while improving process integrity and performance, leading with DNA sequencing. The business leverages expertise in cost-driven optimization of computing from silicon micro-architecture to cluster-level software engineering to build an appliance-deployed service network tied to high-throughput instruments. IAS successfully completed "seed" stage in late 2007 and was funded for first-year operations of $12 million with a peak staff of 17 employees across 5 geographic locations from California to Russia.

Led community/customer-facing aspects of aspects of defining joint research efforts and deploying early access platforms for analytics services to enhance the value and adoption of a new class of radically data-intensive instruments such as second-generation sequencers.

Developed market assessment and segmentation. Constructed phased strategy for business development based on incremental delivery of new capabilities matched to risk and resources. Defined design requirements and positioning from ecosystem analysis and facilitated working sessions with external expert developers at genome centers and research facilities. Represented usage and technical implementation team concerns in meetings with sequencing vendors internationally. Extensive presence at conferences and standards meetings to build network and reputation of Intel in a new field and market.

EXPERIENCE
1992–2007

Strategic Process Development & Platform Architecture **April 2002 to December 2007**

Intel, Channel Platforms Group (CPG) / User Centered Design (UCD)

Worked with Corporate Platform Office to develop the corporate-wide Platform Program Lifecycle. Led architectural strategy for design exploration and product development programs. Presented recommendations and demonstrations to Corporate Technology Council and executive management. Advised Intel Capital on technical diligence and prototyping assessment for components affecting user interface and interaction capabilities. Sponsored university research in computer visual perception/recognition.

Set direction and process for Platform requirements analysis. Piloted processes supporting Platform Planning including system-level analysis, gap identification, and risk reduction by targeted development. Delivered architectural strategy and product requirements for ODM/OEMs.

Led ideation and concept development. Directed multidisciplinary team including industrial design, electrical and thermal/mechanical engineering, channel design research, cost modeling. Presented to nine OD/EMs in Taiwan and Korea to get feedback on how modular concepts would impact existing manufacturing and business models. Worked through Intel Taiwan to ensure account teams understood and supported program & customer visit goals.

Systems Engineer / Quality Liaison, Senior Component Engineer **June 2001 to April 2002**

Intel Corporation, Prescott Design Engineering and Automation

Design engineering on Intel's largest design project to date. Development and support of new tools and techniques for data-driven visualization, analysis, and design; risk and effort projection based directly on design artifacts and design tool output—first such model to exceed predictive levels of statistical correlation.

Liaison to Corporate Quality, facilitating mapping and targeting of risk, cost, effort, and quality measurement, analysis, and improvement. Instrumental in assessing requirements engineering and configuration management, identifying a minimum 25% reduction in headcount for a typical 500-engineer microprocessor design project.

Senior Versatile Engineer **February 2000 to May 2001**

Intel Corporation, Intel®Play™/Smart Toy Lab (joint venture with Mattel)

Leadership role in hardware architecture and development; actively involved in ideation, patent filing, prototyping/simulation, market testing, technology research and feasibility analysis. Architecture and requirements, including safety and other regulatory concerns. Vendor identification, bid package, cost estimation, qualification, and management. Directly collaborated with every other function in the organization.

Senior Software Engineer **May 1999 to February 2000**

Intel Corporation, Home Products Group

Software developer working with mixed open source and proprietary licenses, enhancing and extending Mozilla for set-top boxes running Linux. Participated in external documentation and performance groups, analyzed and planned for target memory goals, and developed cross-platform plug-in support. Built and hosted public automated documentation server integrated with Mozilla project, updated on a nightly basis.

Senior / Horizontal CAD Engineer **May 1996 to May 1999**

Intel Corporation, Design Technology

Technical lead and developer for physical design tools for microprocessor design, with focus on process technology issues including shifting, compaction, and design rule support. Responsible for improvements to product and development process quality. Contributed to architectural definition and capability roadmap for the entire suite of physical design tools. Established automated builds and regressions, code quality metrics, and coding standards.

Senior Software Engineer **May 1995 to May 1996**

Intel Corporation, Internet Technologies Lab

Responsible for identifying and developing Web-based technologies, including the design and deployment of the Corporate Presence Server, www.intel.com. Technical liaison to Corporate Marketing for branding, content, technology, and process-related issues including definition and training. Designed a process for bringing IAL technologies to the public, including testing, documentation, Internet delivery/demonstration, legal/marketing issues. Designed and deployed web-based interactive demonstration to allow visitors to compose and render 3D images on prototype microprocessors; first real-world/public test of new systems based on Pentium® Pro/P6 architecture and silicon.

Senior Design Engineer **July 1992 to May 1995**

Intel Corporation, Microprocessor Division 6

Vertical VLSI Design Engineer responsible for a full design cycle on a number of units including RTL coding, schematic, circuit, timing, layout design, reviews, silicon debug, and supervision on the Pentium® Pro Processor; work proliferated throughout Pentium® II, Pentium® III, Celeron™, Xeon™ server, desktop, and notebook/mobile product lines.

EXPERIENCE 1988–1991

Research Engineer **September 1989 to February 1991**

Microelectronics Research Center, Georgia Institute of Technology

Led engineering & installation of the MiRC's first Electron Beam Nanolithography Facility. Responsible for the design and fabrication of nanometer-scale structures on MBE-grown substrates for exploration of quantum-regime electron device physics. Designed experimental apparatus for precise mechanical insertion of devices into high flux magnetic fields immersed in liquid-helium for testing, measuring femtoampere-scale signals.

Intern Engineer **June 1988 to September 1988**

Tektronix Solid State Research Laboratories

Operation and maintenance of Electron Beam Fabrication. Assisted in design and manufacture of experimental electro-optical devices and in process characterization.

INTEL AWARDS & RECOGNITION

Division Team Award, Corporate Platform Office **January 2008**

PPLC and PLC 2.0 Content and Integration

Recognition for application and improvement of Intel's Corporate Platform and Product Lifecycles.

worldMap "All 'rounder" **January 2008**

For contributions to USFF TOA topic, worldMap process definition, and supporting collateral.

Divisional Recognition Award, Channel Platforms Group **June 2007**

For leadership and contributions in USFF/HDI worldmap topic, and the resulting strategic architectural exploration and prototyping effort.

Intel Software Corporate Quality Network Award **1999**

Corporate-level recognition for web-based automated build, optimization, and quality metrics system.

Divisional Recognition Award, IDC Haifa **June 1998**

Customer award for excellence in product functionality and quality (automated process shifting).

Design Technology / Athena Recognition Award **1998**

For productivity enhancements; improvement to speed of development cycle.

PATENTS

U.S.Patent No. 6536972: Inkjet stylus **March 2003**

U.S.Patent No. 6422775: Digital Messaging Pen **July 2002**

EDUCATION

Master of Science in Electrical Engineering **June 1992**

Georgia Institute of Technology

With research in Electronic Beam Nanolithograhy/CAD and Super-Periodic Quantum-Regime Device Physics

Major: Computer Engineering
Emphasis in Microelectronics, Computer Communications Networks, Digital Signal Processing

Minor: Information and Computer Science
Emphasis in Human-Computer Interfaces, Graphics

Bachelor of Electrical Engineering, High Honor **June 1990**

Georgia Institute of Technology

Certificate Program completed in Computer Engineering

Bachelor of Science in Applied Physics, High Honor **September 1989**

Georgia Institute of Technology

ACTIVITIES & HONORS

Board of Advisors — GenoCAD, Genetic Sequence & Network Design
Visiting Faculty — Virginia Bioinformatics Institute
Ad hoc Reviewer — PLoS ONE
Eta Kappa Nu, Tau Beta Pi — Engineering Honor Societies

Georgia Tech President's Scholar (http://www.psp.gatech.edu/) — Full Academic Scholarship
National Merit Scholar, Georgia Governor's Scholar — Academic Scholarships

CORPORATE PRESENTATIONS

Scenario Planning and *Mobile User Experience*, *Connected Visual Computing* topics **2008**
*world**map**: Global Technology Opportunity*
Scenario planning with senior technologists. Follow-on content development of 3rd generation computing work.

3RD generation computing | Technology Council, TSLRP Demos **2007**
Technology Strategic Long Range Planning (TSLRP)
Presentation of recommendations to senior technologists. Demonstration of high-fidelity experience prototypes.

green t-slrp | modularity for green platforms **2007**
Technology Strategic Long Range Planning (TSLRP)
Represented channel perspectives for modular approaches to reducing product and production footprint on the environment through complete lifecycle analysis.

Density is our Destiny: USFF packaging and HDI technology **2007**
*world**map** topic*
Represented channel perspectives for how to leverage early delivery of dense, cost-effective package technology to reach new markets in the channel. Led resulting program to complete technology development.

User Experience Assessment (UXA) **2006**
Technology Strategic Long Range Planning (TSLRP)
Developed benchmarking data, including interviews of user experience assessment leaders at major technology companies (e.g. Yahoo!). Contributor for key visual communication materials.

Personal Computing Module, Converged Platform **2006**
Corporate Strategic Discussion (CSD)
Led cross-disciplinary aspects to direct and integrate across business exploration, usage-focused, and architectural subteams. Resulted in roadmap changes to converge desktop and mobile silicon & platforms.

Neutrino / Process Shifting **1998**
Intel Design and Test Technology Conference (DTTC)
Selected as keynote demonstration presenter for DTTC by Microprocessor Group Vice President.

PUBLICATIONS & TALKS

Santa Fe Institute Business Network, *25th Anniversary Symposium* **November 2008**
"Open Questions in Science, Technology and Business" Invited speaker: *design | complexity*
http://www.santafe.edu/events/workshops
Presented on challenging issues of complexity for the next quarter-century. The talk outlined the complexity in microprocessor designs and the methods and organizations that design them, and emerging parallels in biotech.

Journal: Trends in Biology **October 2008**
Position Paper: *Rising Above the Sequence.*
Co-author with Berkeley and Virginia Bioinformatics Institute on VLSI-inspired approaches to Synthetic Biology.

Intel Technology Journal, *Designing Technology with People in Mind* **February 2007**
Paper: *Intel® Usage-to-Platform Requirements Process.*
Co-author of externally published whitepaper describing methods and process used to support requirements engineering in Platform Planning developed by User Centered Design.

Intel Innovation Forum **October 2005**
Posters, Brochure: *ingredients to platforms, PPLC exploration*
Collateral development and information graphics support for Corporate Platform Office presentation.

Intel Design and Test Technology Conference (DTTC) **April 2003**
Paper/Poster: *Augmenting Timing Convergence with Risk/Effort-based Analysis*

Emergent Engineering Workshop, MIT Media Lab Center of Bits and Atoms **October 2002**
http://cba.media.mit.edu/events/02.10.emergent/
Invited speaker on billion transistor microprocessor design and limits of engineering complexity.

Intel Engineering Computing Technology Conference (ECTC) **April 2002**
Paper: *Managing Roles, Workflows, and Information through Content Management Frameworks*
Co-author of paper outlining workflow tools and methods to address the needs of silicon design projects.