BRIAN W. BRAMLETT

Portland, Oregon
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OBJECTIVE   Develop a career with a progressive organization in the areas of product design, architecture and engineering, with particular emphasis on user-based and system-level design.

SKILLS   **Software Design and Engineering**

Systems, Architecture, and Algorithms	*Human-Computer Interfaces.*
Computer communication networks, media, protocols.	3D modeling and rendering.
Multidimensional DSP.	Visualization of complex information.
Queueing theory.	Web design, development, support.
Digital processing of speech signals.	Computer-based graphic design.
Parallel computer architectures and programming.	Design for human perception.
Object-oriented design.	
Digital arithmetic.	*Languages / Environments*
(EDA) CAD Framework design.	C, C++, PERL, Unix Shells, Assembly.
Computationally distributed systems, scheduling.	Java, D/HTML, JavaScript.
Client/Server interactive systems.	Linux, AIX, HP-UX, FreeBSD.
Software engineering	*Tools and Libraries*
Professional development and engineering practices.	OpenGL / MESA, X, GTK
Validation and verification.	CGI, GNU and Cygnus tools, CVS/RCS.
Object-oriented design and programming.	

EDUCATION   **Master of Science in Electrical Engineering**   **June 1992**
Georgia Institute of Technology

Major: Computer Engineering
    Emphasis in Microelectronics, Computer Communications Networks, Digital Signal Processing

Minor: Information and Computer Science
    Emphasis in Human-Computer interfaces, Graphics

Research in Electronic Beam Nanolithograhy/CAD and Super-Periodic Quantum Device Physics

Bachelor of Electrical Engineering, High Honor   **June 1990**
Georgia Institute of Technology

Certificate Program completed in Computer Engineering

Bachelor of Science in Applied Physics, High Honor   **September 1989**
Georgia Institute of Technology

HONORS

Eta Kappa Nu	Electrical Engineering Honor Society
Tau Beta Pi	Engineering Honor Society
Georgia Tech President's Scholar (www.enrollment.gatech.edu/psp)	Academic Scholarship
National Merit Scholar	Academic Scholarship
Georgia Governor's Scholar	Academic Scholarship

EXPERIENCE	**Senior Software Engineer**	**May 1999 to present**

Intel Corporation, Home Products Group/HPG Software Engineering, Hillsboro, Oregon
Software developer working with mixed open source and proprietary licenses, enhancing and extending Mozilla (Netscape's open source browser project) for set-top boxes running Linux under a wide range of memory requirements and functional capabilities. Participated in external documentation and performance groups, analysed and planned for target memory goals, and developed cross-platform plug-in support from Linux.

Senior / Horizontal CAD Engineer   **May 1997 to May 1999**
Intel Corporation, Design Technology/Athena Group, Hillsboro, Oregon
Technical lead and developer for physical design tools for microprocessor design, with focus on process technology issues including shifting, compaction, and design rule support. Responsible for improvements to product and development process quality. Contributed to architectural definition and capability roadmap for the entire suite of physical design tools. Established automated builds and regressions, code quality metrics, and coding standards. Trained as a review moderator.

Senior CAD Engineer   **May 1996 to May 1997**
Intel Corporation, Design Technology/Athena Group, Hillsboro, Oregon
Verification and validation of tools in the domains of full chip layout and physical design, and logic and formal verification. Generated specifications and standards for software testing, quality requirements for tool behavior and documentation, and flow-level test plans.

Senior Software Engineer   **February 1996 to May 1996**
Intel Corporation, Software Tools and Integration Lab, Hillsboro, Oregon
Responsible for designing an architecture and process for bringing IAL technologies from the labs to Intel and the public, including testing, documentation, packaging, Internet delivery and demonstration, legal and marketing issues.

Senior Software Engineer   **May 1995 to January 1996**
Intel Corporation, Internet Technologies Lab, Hillsboro, Oregon
Responsible for identifying and developing Web-based technologies, including the design and deployment of the Corporate Presence Server, www.intel.com. Technical liaison to Corporate Marketing and the CPS Team for content, technology, and process-related issues. Designed, developed, and deployed web-based interactive demonstration to allow visitors to compose and render 3D images on prototype microprocessors.

Senior Design Engineer   **July 1992 to May 1995**
Intel Corporation, Microprocessor Division 6, Hillsboro, Oregon
Vertical VLSI Design Engineer responsible for a full design cycle on a number of units including RTL coding, schematic, circuit, timing, layout design, reviews, silicon debug, and supervision on the Pentium Pro Processor.

Research Engineer   **September 1989 to February 1991**
Microelectronics Research Center, Georgia Institute of Technology
Design, installation, management, and maintenance of the Scanning Electron Microscope Electron Beam Nanolithography Facility. Design and fabrication of nanometer-scale structures on MBE-grown substrates for exploration of quantum electron device physics. Design and construction of low temperature, high magnetic field sample probes.

Intern Engineer   **June 1988 to September 1988**
Tektronix Solid State Research Laboratories, Beaverton, Oregon
Operation and maintenance of Electron Beam Fabrication. Assisted in design and manufacture of experimental electro-optical devices and in process characterization.

INTEL AWARDS	Software Corporate Quality Network Award, 1999 (http://swcqn.intel.com/award/)

Corporate-level recognition for web-based automated build, optimization, and quality metrics system.

Divisional Recognition Award, IDC Haifa, June 1998
Customer award for excellence in product functionality and quality (automated process shifting).

ASSOCIATIONS	ACM
	IEEE