What Is RCU?

Indian Institute of Science, Bangalore
Overview

- Mutual Exclusion
- Example Application
- Performance of Synchronization Mechanisms
- Making Software Live With Current (and Future) Hardware
- Implementing RCU
- RCU Grace Periods: Conceptual and Graphical Views
- Performance
- RCU Area of Applicability
- Summary
Mutual Exclusion

• “We simply do not have a synchronization mechanism that can enforce mutual exclusion”

• True or false?
Example Application
Example Application

- Schrödinger wants to construct an in-memory database for the animals in his zoo (example in upcoming ACM Queue)
  - Births result in insertions, deaths in deletions
  - Queries from those interested in Schrödinger's animals
  - Lots of short-lived animals such as mice: High update rate
  - Great interest in Schrödinger's cat (perhaps queries from mice?)
Example Application: Schrödinger's Cat

BEING SIMULTANEOUSLY DEAD AND ALIVE IN THE BOX GAVE ME AN INCREDIBLE PERSPECTIVE OVER THE "LIFE, THE UNIVERSE AND EVERYTHING". AND I AM HERE TO TELL IT TO THE WORLD!
Example Application

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  - Births result in insertions, deaths in deletions
  - Queries from those interested in Schrödinger's animals
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  - Great interest in Schrödinger's cat (perhaps queries from mice?)

- Simple approach: chained hash table with per-bucket locking

```
0: lock  →  mouse  →  zebra
1: lock  →  boa     →  cat     →  gnu
2: lock
3: lock
```
Example Application

- Schrödinger wants to construct an in-memory database for the animals in his zoo (example in upcoming ACM Queue)
  - Births result in insertions, deaths in deletions
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- Simple approach: chained hash table with per-bucket locking

![Diagram of chained hash table]

Will holding this lock prevent the cat from dying?
Read-Only Bucket-Locked Hash Table Performance

Why the dropoff???

Lookups per Millisecond

Number of CPUs/Threads

2GHz Intel Xeon Westmere-EX, 1024 hash buckets
Varying Number of Hash Buckets

2GHz Intel Xeon Westmere-EX

Still a dropoff...

Number of CPUs/Threads

Lookup per Millisecond

16384
8192
4096
2048
1024
NUMA Effects???

- `/sys/devices/system/cpu/cpu00/cache/index0/shared_cpu_list: 0,32`
- `/sys/devices/system/cpu/cpu00/cache/index1/shared_cpu_list: 0,32`
- `/sys/devices/system/cpu/cpu00/cache/index2/shared_cpu_list: 0,32`
- `/sys/devices/system/cpu/cpu00/cache/index3/shared_cpu_list: 0-7,32-39`

- Two hardware threads per core, eight cores per socket
- Try using only one CPU per socket: CPUs 0, 8, 16, and 24
Bucket-Locked Hash Performance: 1 CPU/Socket

2GHz Intel Xeon Westmere-EX: This is not the sort of scalability Schrödinger requires!!!
Performance of Synchronization Mechanisms
## Performance of Synchronization Mechanisms

### 16-CPU 2.8GHz Intel X5550 (Nehalem) System

<table>
<thead>
<tr>
<th>Operation</th>
<th>Cost (ns)</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock period</td>
<td>0.4</td>
<td>1</td>
</tr>
<tr>
<td>“Best-case” CAS</td>
<td>12.2</td>
<td>33.8</td>
</tr>
<tr>
<td>Best-case lock</td>
<td>25.6</td>
<td>71.2</td>
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<tr>
<td>Single cache miss</td>
<td>12.9</td>
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<td>CAS cache miss</td>
<td>7.0</td>
<td>19.4</td>
</tr>
<tr>
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<td>31.2</td>
<td>86.6</td>
</tr>
<tr>
<td>CAS cache miss (off-core)</td>
<td>31.2</td>
<td>86.5</td>
</tr>
<tr>
<td>Single cache miss (off-socket)</td>
<td>92.4</td>
<td>256.7</td>
</tr>
<tr>
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<td>95.9</td>
<td>266.4</td>
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And these are best-case values!!! (Why?)
Why All These Low-Level Details???

• Would you trust a bridge designed by someone who did not understand strengths of materials?
  – Or a ship designed by someone who did not understand the steel-alloy transition temperatures?
  – Or a house designed by someone who did not understand that unfinished wood rots when wet?
  – Or a car designed by someone who did not understand the corrosion properties of the metals used in the exhaust system?
  – Or a space shuttle designed by someone who did not understand the temperature limitations of O-rings?

• So why trust algorithms from someone ignorant of the properties of the underlying hardware???
But What Do The Operation Timings Really Mean???
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- Single-instruction critical sections protected by multiple locks

Uncontended

Contended, No Spinning

So, what does this mean?
But What Do The Operation Timings Really Mean???

- Single-instruction critical sections protected by multiple locks

Uncontended

256.7 cycles

1 cycle

258 CPUs to break even with single CPU!

Contended, No Spinning

256.7 cycles

1 cycle

514 CPUs to break even with single CPU!!!
But What Do The Operation Timings Really Mean???

- Single-instruction critical sections protected by multiple locks

Uncontended

Contended, No Spinning

Contended, Spinning

Arbitrarily large number of CPUs to break even with single CPU!!!
Reader-Writer Locks Are Even Worse!
Reader-Writer Locks Are Even Worse!

800 CPUs to break even with a single CPU!!!
But What About Scaling With Atomic Operations?
If You Think Single Atomic is Expensive, Try Lots!!!
Why So Slow???
System Hardware Structure and Laws of Physics

Electrons move at 0.03C to 0.3C in transistors and, so lots of waiting. 3D???
Atomic Increment of Global Variable

Lots and Lots of Latency!!!
Atomic Increment of Per-CPU Counter

Little Latency, Lots of Increments at Core Clock Rate
Can't The Hardware Do Better Than This???
SGI systems used this approach in the 1990s, expect modern micros to pick it up. Still not as good as per-CPU counters.
Problem With Physics #1: Finite Speed of Light
Problem With Physics #2: Atomic Nature of Matter

Source

No complaints for eons, and now, suddenly, we're too #**#$ big!?!?

I feel so fat!

Base

And our dielectric constant isn't bold enough for them! They can go find some other #$**$ atom! Sheesh!
How Can Software Live With This Hardware???
Design Principle: Avoid Bottlenecks

Only one of something: bad for performance and scalability. Also typically results in high complexity.
Design Principle: Avoid Bottlenecks

Many instances of something good!
Avoiding tightly coupled interactions is an excellent way to avoid bugs. But NUMA effects defeated this for per-bucket locking!!!
### Design Principle: Avoid Expensive Operations

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**Notes:**
- Need to be here! (Partitioning/RCU)
- Heavily optimized reader-writer lock might get here for readers (but too bad about those poor writers...)
- Typical synchronization mechanisms do this a lot
Design Principle: Get Your Money's Worth

- If synchronization is expensive, use large critical sections
- On Nehalem, off-socket CAS costs about 260 cycles
  - So instead of a single-cycle critical section, have a 26000-cycle critical section, reducing synchronization overhead to about 1%
- Of course, we also need to keep contention low, which usually means we want short critical sections
  - Resolve this by applying parallelism at as high a level as possible
  - Parallelize entire applications rather than low-level algorithms!
Design Principle: Avoid Mutual Exclusion!!!

Dead Time!!!
Design Principle: Avoiding Mutual Exclusion

No Dead Time!
But How Can This Possibly Be Implemented???
Implementing RCU

- Lightest-weight conceivable read-side primitives
Implementing RCU

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  - /* Assume non-preemptible (run-to-block) environment. */
  - #define rcu_read_lock()
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- How can something that does not affect machine state be used as a synchronization primitive???
What Is RCU?

- Publishing of new data
- Subscribing to the current version of data
- Waiting for pre-existing RCU readers: Avoid disrupting readers by maintaining multiple versions of the data
  - Each *reader* continues traversing its *copy* of the data while a new *copy* might be being created concurrently by each *updater*
    - Hence the name *read-copy update*, or RCU
  - Once all pre-existing RCU readers are done with them, old versions of the data may be discarded
Publication of And Subscription to New Data

Key:
- Pink: Dangerous for updates: all readers can access
- Yellow: Still dangerous for updates: pre-existing readers can access (next slide)
- Green: Safe for updates: inaccessible to all readers

```
cptr
->a=?
->b=?
->c=?
```

```
cptr
->a=1
->b=2
->c=3
```
Memory Ordering: Mischief From Compiler and CPU
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- Original updater code:
  ```c
  p = malloc(sizeof(*p));
  p->a = 1;
  p->b = 2;
  p->c = 3;
  cptr = p;
  ```

- Original reader code:
  ```c
  p = cptr;
  foo(p->a, p->b, p->c);
  ```

- Mischievous updater code:
  ```c
  p = malloc(sizeof(*p));
  cptr = p;
  p->a = 1;
  p->b = 2;
  p->c = 3;
  ```

- Mischievous reader code:
  ```c
  retry:
  p = guess(cptr);
  foo(p->a, p->b, p->c);
  if (p != cptr)
    goto retry;
  ```
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  if (p != cptr)
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But don't take my word for it on HW value speculation:
http://www.openvms.compaq.com/wizard/wiz_2637.html
Preventing Memory-Order Mischief

- Updater uses `rcu_assign_pointer()` to publish pointer:
  
  ```c
  #define rcu_assign_pointer(p, v) (
    ({
        smp_wmb(); /* SMP Write Memory Barrier */ 
        (p) = (v); 
    })
  )
  ```

- Reader uses `rcu_dereference()` to subscribe to pointer:
  
  ```c
  #define rcu_dereference(p) (
    ({
        typeof(p) _p1 = (*(volatile typeof(p)*)&(p)); 
        smp_read_barrier_depends(); 
        _p1; 
    })
  )
  ```

- The Linux-kernel definitions are more ornate: Debugging code
Preventing Memory-Order Mischief

“Memory-order-mischief proof” updater code:
```c
p = malloc(sizeof(*p));
p->a = 1;
p->b = 2;
p->c = 3;
rpu_assign_pointer(cptr, p);
```

“Memory-order-mischief proof” reader code:
```c
p = rcu_dereference(cptr);
foo(p->a, p->b, p->c);
```
But if all we do is add, we have a big memory leak!!!
RCU Removal From Linked List

- Combines waiting for readers and multiple versions:
  - Writer removes the cat's element from the list (list_del_rcu())
  - Writer waits for all readers to finish (synchronize_rcu())
  - Writer can then free the cat's element (kfree())
RCU Removal From Linked List

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  - Writer can then free the cat's element (kfree())

But if readers leave no trace in memory, how can we possibly tell when they are done???
How Can RCU Tell When Readers Are Done???
How Can RCU Tell When Readers Are Done???

That is, without re-introducing all of the overhead and latency inherent to other synchronization mechanisms...
But First, Some RCU Nomenclature

- **RCU read-side critical section**
  - Begins with `rcu_read_lock()`, ends with `rcu_read_unlock()`, and may contain `rcu_dereference()`

- **Quiescent state**
  - Any code that is not in an RCU read-side critical section

- **Extended quiescent state**
  - Quiescent state that persists for a significant time period

- **RCU grace period**
  - Time period when every thread was in at least one quiescent state
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- OK, names are nice, but how can you possibly implement this???
Waiting for Pre-Existing Readers: QSBR

- Non-preemptive environment (CONFIG_PREEMPT=n)
  - RCU readers are not permitted to block
  - Same rule as for tasks holding spinlocks
Waiting for Pre-Existing Readers: QSBR

- Non-preemptive environment (CONFIG_PREEMPT=n)
  - RCU readers are not permitted to block
  - Same rule as for tasks holding spinlocks

- CPU context switch means all that CPU's readers are done

- Grace period ends after all CPUs execute a context switch
Synchronization Without Changing Machine State???

- But rcu_read_lock() does not need to change machine state
  - Instead, it acts on the developer, who must avoid blocking within RCU read-side critical sections
  - Or, more generally, avoid quiescent states within RCU read-side critical sections
Synchronization Without Changing Machine State???

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- RCU is therefore synchronization via social engineering
Synchronization Without Changing Machine State???

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  - Or, more generally, avoid quiescent states within RCU read-side critical sections

- RCU is therefore synchronization via social engineering

- Just as is the case for most synchronization mechanisms
  - “Avoid data races”
  - “Protect specified variables with the corresponding lock”
  - “Access shared variables only within transactions”
Toy Implementation of RCU: 20 Lines of Code

- **Read-side primitives:**
  ```c
  #define rcu_read_lock()
  #define rcu_read_unlock()
  #define rcu_dereference(p) \ 
  ({ \ 
      typeof(p) _p1 = (*(volatile typeof(p)*)&(p)); \ 
      smp_read_barrier_depends(); \ 
      _p1; \ 
  })
  ```

- **Update-side primitives**
  ```c
  #define rcu_assign_pointer(p, v) \ 
  ({ \ 
      smp_wmb(); \ 
      (p) = (v); \ 
  })
  void synchronize_rcu(void)
  {
    int cpu;
    for_each_online_cpu(cpu) \ 
      run_on(cpu);
  }
  ```
Tooy Implementation of RCU: 20 Lines of Code

- **Read-side primitives:**
  
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  #define rcu_read_lock()
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  })
  ```

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  #define rcu_assign_pointer(p, v) ({
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  })
  ```

  ```c
  void synchronize_rcu(void)
  {
    int cpu;
    for_each_online_cpu(cpu)
      run_on(cpu);
  }
  ```

  Only 9 of which are needed on SC systems...
  And some people still insist that RCU is complicated... ;-)
Complex Atomic-To-Reader Updates
RCU Replacement Of Item In Linked List
RCU Grace Periods: Conceptual and Graphical Views
RCU Grace Periods: A Conceptual View

- **RCU read-side critical section**
  - Begins with rcu_read_lock(), ends with rcu_read_unlock(), and may contain rcu_dereference()

- **Quiescent state**
  - Any code that is not in an RCU read-side critical section

- **Extended quiescent state**
  - Quiescent state that persists for a significant time period

- **RCU grace period**
  - Time period when every thread is in at least one quiescent state
  - Ends when all pre-existing readers complete
  - Guaranteed to complete in finite time iff all RCU read-side critical sections are of finite duration

- But what happens if you try to extend an RCU read-side critical section across a grace period?
So what happens if you try to extend an RCU read-side critical section across a grace period?
A grace period is not permitted to end until all pre-existing readers have completed.
But it is OK for RCU to be lazy and allow a grace period to extend longer than necessary
And it is also OK for RCU to be even more lazy and start a grace period later than necessary.

But why is this useful?
Starting a grace period late can allow it to serve multiple updates, decreasing the per-update RCU overhead. But...
The Costs and Benefits of Laziness

- Starting the grace period later increases the number of updates per grace period, reducing the per-update overhead.
- Delaying the end of the grace period increases grace-period latency.
- Increasing the number of updates per grace period increases the memory usage.
  - Therefore, starting grace periods late is a good tradeoff if memory is cheap and communication is expense, as is the case in modern multicore systems.
    • And if real-time threads avoid waiting for grace periods to complete.
  - However...
And it is OK for the system to complain (or even abort) if a grace period extends too long. Too-long of grace periods are likely to result in death by memory exhaustion anyway.
RCU Asynchronous Grace-Period Detection
RCU Asynchronous Grace-Period Detection

- The call_rcu() function registers an RCU callback, which is invoked after a subsequent grace period elapses.

API:

```c
void (*func)(struct rcu_head *rcu);
```

- The rcu_head structure:

```c
struct rcu_head {
    struct rcu_head *next;
    void (*func)(struct rcu_head *rcu);
};
```

- The rcu_head structure is normally embedded within the RCU-protected data structure.
RCU Grace Period: An Asynchronous Graphical View

```
call_rcu(&p->rcu, func);
call_rcu(&p->rcu, func);

func(&p->rcu);
func(&p->rcu);
```
Performance
Theoretical Performance

RCU (wait-free) → 1 cycle → Full performance, linear scaling, real-time response

Uncontended
- 71.2 cycles
- 1 cycle

Contended, No Spinning
- 71.2 cycles
- 1 cycle
- 71.2 cycles

73 CPUs to break even with a single CPU!

144 CPUs to break even with a single CPU!!!
Measured Performance
Schrödinger's Zoo: Read-Only

RCU and hazard pointers scale quite well!!!
Schrödinger's Zoo: Read-Only Cat-Heavy Workload

RCU handles locality quite well, hazard pointers not bad, bucket locking horribly
Real-Time Response to Changes
RCU vs. Reader-Writer-Lock Real-Time Latency

External Event

RCU Latency

rwlock Latency
RCU Performance: “Free is a Very Good Price!!!”
RCU Performance: “Free is a Very Good Price!!!”
And Nothing Is Faster Than Doing Nothing!!!
Schrodinger’s zoo is in blue: Can’t tell exactly when an animal is born or dies anyway! Plus, no lock you can hold will prevent an animal’s death...
RCU Applicability to the Linux Kernel
Summary
Summary

- Synchronization overhead is a big issue for parallel programs
- Straightforward design techniques can avoid this overhead
  - Partition the problem: “Many instances of something good!”
  - Avoid expensive operations
  - Avoid mutual exclusion
- RCU is part of the solution
  - Excellent for read-mostly data where staleness and inconsistency OK
  - Good for read-mostly data where consistency is required
  - Can be OK for read-write data where consistency is required
  - Might not be best for update-mostly consistency-required data
  - Used heavily in the Linux kernel
- Much more information on RCU is available...
To Probe Further:

- https://queue.acm.org/detail.cfm?id=2488549
  - “Structured Deferral: Synchronization via Procrastination”
- http://doi.ieeecomputersociety.org/10.1109/TPDS.2011.159 and
  http://www.computer.org/cms/Computer.org/dl/trans/td/2012/02/extras/ttd2012020375s.pdf
  - “User-Level Implementations of Read-Copy Update”
- git://lttng.org/userspace-rcu.git (User-space RCU git tree)
  - Applying RCU and weighted-balance tree to Linux mmap_sem.
  - RCU-protected resizable hash tables, both in kernel and user space
  - Combining RCU and software transactional memory
- http://wiki.cs.pdx.edu/rp/: Relativistic programming, a generalization of RCU
- http://lwn.net/Articles/262464/, http://lwn.net/Articles/263130/, http://lwn.net/Articles/264090/
  - “What is RCU?” Series
  - RCU motivation, implementations, usage patterns, performance (micro+sys)
  - System-level performance for SELinux workload: >500x improvement
  - Comparison of RCU and NBS (later appeared in JPDC)
- http://doi.acm.org/10.1145/1400097.1400099
  - History of RCU in Linux (Linux changed RCU more than vice versa)
  - Harvard University class notes on RCU (Courtesy Eddie Koher)
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Questions?

Use the right tool for the job!!!