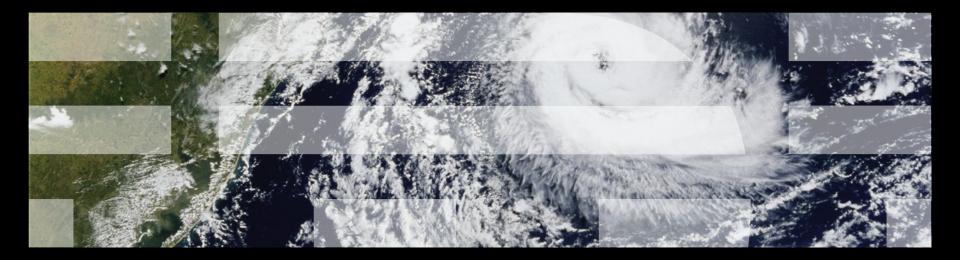


# Validating Core Parallel Software





#### **Overview**

- Who is Paul and How Did He Get This Way?
- Avoiding Debugging By Design
- Avoiding Debugging By Process
- Avoiding Debugging By Mechanical Proofs
- Avoiding Debugging By Statistical Analysis
- Coping With Schedule Pressure
- But I Did All This And There Are Still Bugs!!!
- Summary and Conclusions



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- Grew up in rural Oregon
- First use of computer in high school (72-76)
   –IBM mainframe: punched cards and FORTRAN
   –Later ASR33 TTY and BASIC
- BSME & BSCS, Oregon State University (76-81)
   Tuition provided by FORTRAN and COBOL
- Contract Programming and Consulting (81-85)
  - -Building control system (Pascal on z80)
  - -Security card-access system (Pascal on PDP-11)
  - -Dining hall system (Pascal on PDP-11)
  - -Acoustic navigation system (C on PDP-11)



SRI International (85-90)

- -UNIX systems administration
- -Packet-radio research
- -Internet protocol research

#### Sequent Computer Systems (90-00)

- -Communications performance
- -Memory allocators, TLB, RCU, timers, ...
- IBM LTC (00-present)
  - -NUMA-aware and brlock-like locking primitive in AIX
    - They didn't want RCU
  - -RCU maintainer for Linux kernel



I have never:

- -Used kprobes or SystemTap to find a bug
- -Taken a core dump from a Linux system
- -Used ftrace to find a bug
- -Used "perf" at all

#### I sometimes:

- -Use debugging printk()s
- -Use event tracing
- -Use WARN\_ON\_ONCE()
  - Probably more often than printk()
- l often:
  - -Use special-purpose counters

Why avoid these debug techniques? What to do instead?



# Avoiding Debugging By Design

7

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# **Avoiding Debugging By Design**

- Understand the Hardware
- Understand the Software Environment



#### 4-CPU 1.8GHz AMD Opteron 844 system

Need to be here! Cost (ns) Operation Ratio (Partitioning/RCU) Clock period 0.6**Best-case CAS** 37.9 63.2 **Best-case** lock 65.6 109.3 Single cache miss 139.5 232.5 CAS cache miss 306.0 510.0

Heavily optimized readerwriter lock might get here for readers (but too bad about those poor writers...)



Typical synchronization mechanisms do this a lot



#### 4-CPU 1.8GHz AMD Opteron 844 system

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#### But this is an old system...



Typical synchronization mechanisms do this a lot



#### 4-CPU 1.8GHz AMD Opteron 844 system

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Heavily optimized readerwriter lock might get here for readers (but too bad about those poor writers...)

# But this is an old system...



Typical synchronization mechanisms do this a lot

# And why low-level details???



#### Why All These Low-Level Details???

- Would you trust a bridge designed by someone who did not understand strengths of materials?
  - –Or a ship designed by someone who did not understand the steel-alloy transition temperatures?
  - -Or a house designed by someone who did not understand that unfinished wood rots when wet?
  - -Or a car designed by someone who did not understand the corrosion properties of the metals used in the exhaust system?
  - -Or a space shuttle designed by someone who did not understand the temperature limitations of O-rings?
- So why trust algorithms from someone ignorant of the properties of the underlying hardware???



#### **But Isn't Hardware Just Getting Faster?**



16-CPU 2.8GHz Intel X5550 (Nehalem) System

| Operation         | Cost (ns) | Ratio |
|-------------------|-----------|-------|
| Clock period      | 0.4       | 1     |
| "Best-case" CAS   | 12.2      | 33.8  |
| Best-case lock    | 25.6      | 71.2  |
| Single cache miss | 12.9      | 35.8  |
| CAS cache miss    | 7.0       | 19.4  |

# What a difference a few years can make!!!



#### 16-CPU 2.8GHz Intel X5550 (Nehalem) System

| Operation                    | Cost (ns) | Ratio |
|------------------------------|-----------|-------|
| Clock period                 | 0.4       | 1     |
| "Best-case" CAS              | 12.2      | 33.8  |
| Best-case lock               | 25.6      | 71.2  |
| Single cache "miss"          | 12.9      | 35.8  |
| CAS cache "miss"             | 7.0       | 19.4  |
| Single cache miss (off-core) | 31.2      | 86.6  |
| CAS cache miss (off-core)    | 31.2      | 86.5  |

Not *quite* so good... But still a 6x improvement!!!

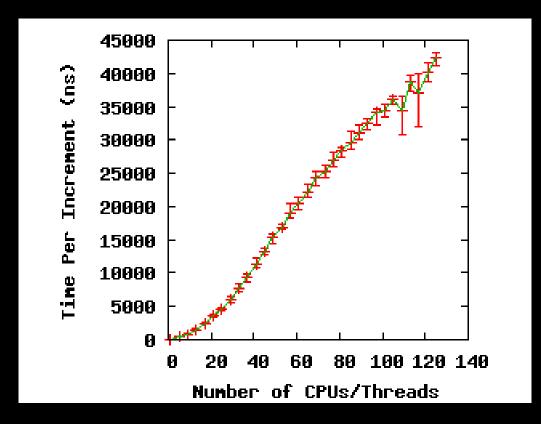


#### 16-CPU 2.8GHz Intel X5550 (Nehalem) System

| Operation                      | Cost (ns) | Ratio |
|--------------------------------|-----------|-------|
| Clock period                   | 0.4       | 1     |
| "Best-case" CAS                | 12.2      | 33.8  |
| Best-case lock                 | 25.6      | 71.2  |
| Single cache miss              | 12.9      | 35.8  |
| CAS cache miss                 | 7.0       | 19.4  |
| Single cache miss (off-core)   | 31.2      | 86.6  |
| CAS cache miss (off-core)      | 31.2      | 86.5  |
| Single cache miss (off-socket) | 92.4      | 256.7 |
| CAS cache miss (off-socket)    | 95.9      | 266.4 |

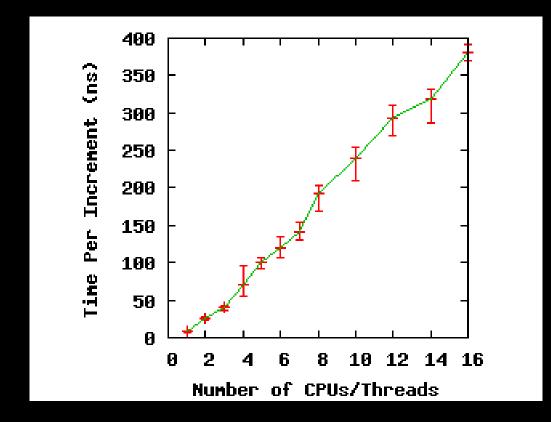
Maybe not such a big difference after all... And these are best-case values!!! (Why?)





If you thought a *single* atomic operation was slow, try lots of them!!! (Parallel atomic increment of single variable on 1.9GHz Power 5 system)

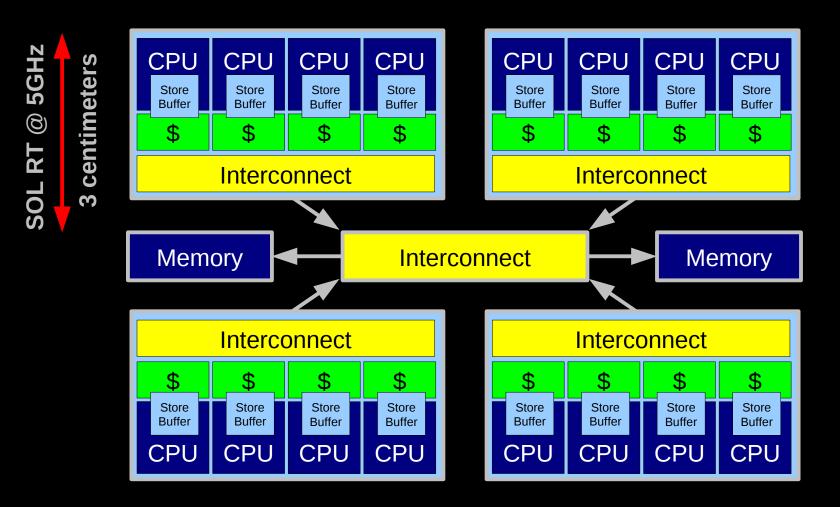




Same effect on a 16-CPU 2.8GHz Intel X5550 (Nehalem) system



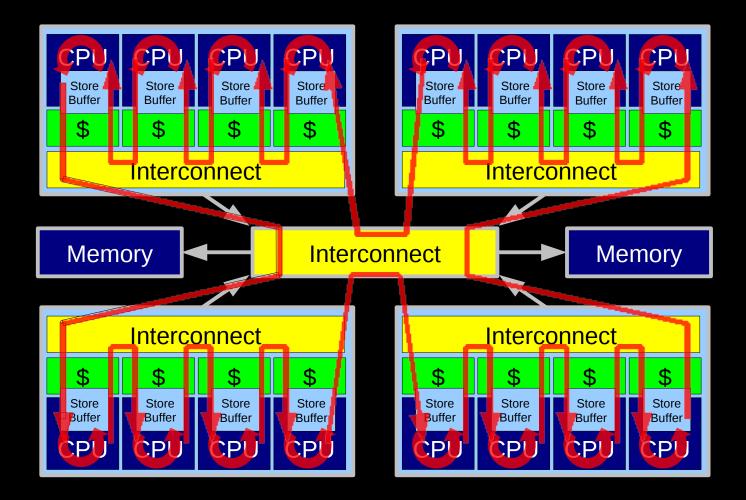
#### **System Hardware Structure**



Electrons move at 0.03C to 0.3C in transistors and, so lots of waiting. 3D???



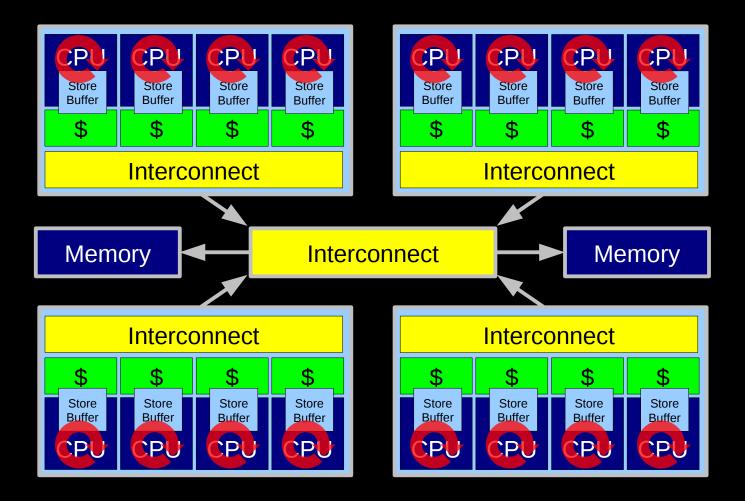
#### **Atomic Increment of Global Variable**



Lots and Lots of Latency!!!



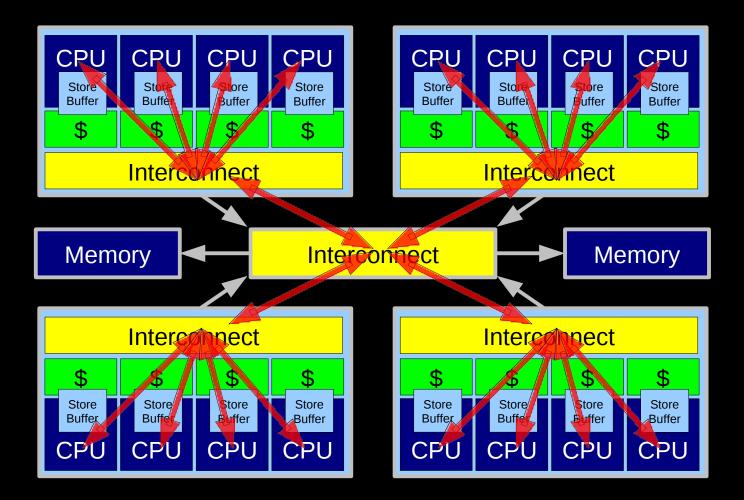
#### **Atomic Increment of Per-CPU Variable**



Little Latency, Lots of Increments at Core Clock Rate

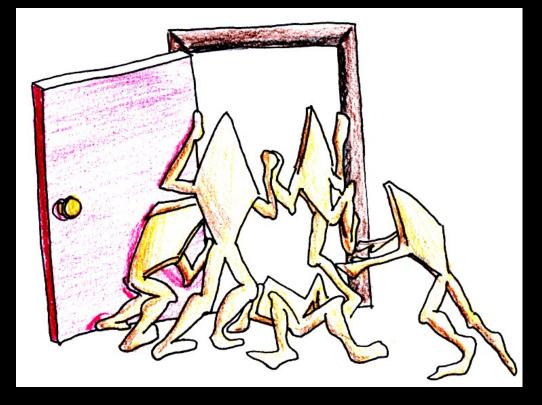


#### **HW-Assist Atomic Increment of Global Variable**





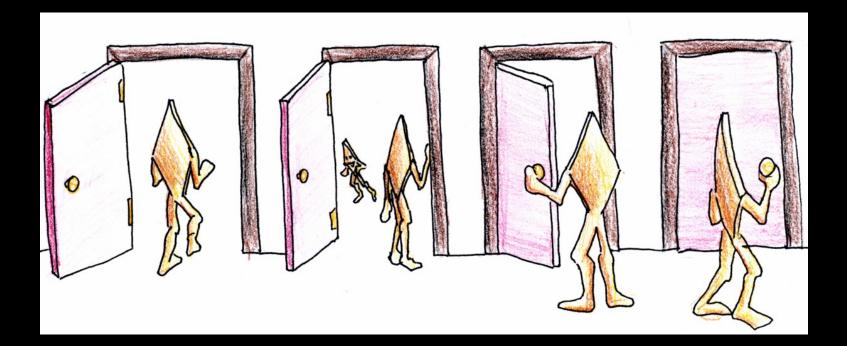
#### **Design Principle: Avoid Bottlenecks**



Only one of something: bad for performance and scalability



#### **Design Principle: Avoid Bottlenecks**



Many instances of something good! Any exceptions to this rule?



#### **Understand the Hardware: Summary**

- A strong understanding of the hardware helps rule out infeasible designs early in process
- Understanding hardware trends helps reduce the amount of future rework required
- Ditto for low-level software that your code depends on



#### **Understand the Software Environment**

Understand the Workloads

-Which for Linux means a great many of them

-Your code must take whatever shows up

Google-Search LWN

-But you knew this already

#### Test Unfamiliar Primitives

- -And complain on LKML if they break
- -Preferably accompanying the complaint with a fix

Review Others' Code

-See recent ltc-interlock discussion for how-to info

#### Make a Map

-See next slides...



## Making a Map of Software



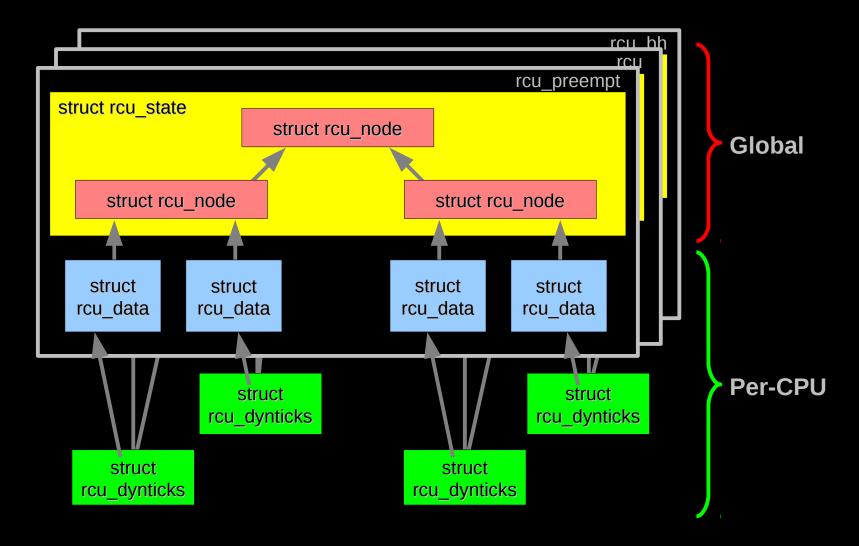
#### **Hierarchical RCU Data Structures**

1 struct rcu dynticks { int dynticks\_nesting; 2 3 int dynticks; int dynticks\_nmi; 4 5 }; 6 7 struct rcu node { spinlock\_t lock; 8 9 long gpnum; long completed; 10 11unsigned long gsmask; 12 unsigned long gsmaskinit; 13 unsigned long grpmask; 14 int grplo; 15 int grphi; 16 u8 grpnum; 17 u8 level; struct rcu\_node \*parent; 18 19 struct list head blocked tasks[2]; 20 } 21 22 struct rcu\_data { 23 long completed; 24 long gpnum; 25 long passed\_quiesc\_completed; 26 bool passed\_quiesc; 27 bool as pending; 28 bool beenonline; 29 preemptable; bool struct rcu\_node \*mynode; 30 31 unsigned long grpmask; 32 struct rcu\_head \*nxtlist; 33 struct rcu\_head \*\*nxttail[RCU\_NEXT\_SIZE]; 34 long glen; 35 glen\_last\_fqs\_check; lona 36 unsigned long n\_force\_qs\_snap; 37 blimit; long 38 #ifdef CONFIG NO HZ 39 struct rcu\_dynticks \*dynticks; 40 int dynticks\_snap; 41 int dynticks\_nmi\_snap;

42 #ifdef CONFIG NO HZ 43 unsigned long dynticks\_fqs; 44 #endif /\* #ifdef CONFIG NO HZ \*/ unsigned long offline fgs; 45 unsigned long resched ipi; 46 47 long n\_rcu\_pending; 48 long n\_rp\_qs\_pending; 49 long n\_rp\_cb\_ready; 50 long n\_rp\_cpu\_needs\_gp; 51 long n\_rp\_gp\_completed; 52 long n\_rp\_gp\_started; 53 long n\_rp\_need\_fqs; 54 long n\_rp\_need\_nothing; 55 int cpu; 56 }; 57 58 struct rcu\_state { 59 struct rcu node node[NUM RCU NODES]; struct rcu node \*level[NUM RCU LVLS]; 60 u32 levelcnt[MAX\_RCU\_LVLS + 1]; 61 62 u8 levelspread[NUM\_RCU\_LVLS]; 63 struct rcu\_data \*rda[NR\_CPUS]; 64 u8 signaled; 65 long gpnum; 66 long completed; 67 spinlock\_t onofflock; 68 struct rcu\_head \*orphan\_cbs\_list; 69 struct rcu head \*\*orphan cbs tail; 70 long orphan\_glen; 71 spinlock\_t fqslock; 72 unsigned long jiffies\_force\_qs; 73 unsigned long n\_force\_qs; unsigned long n\_force\_qs\_lh; 74 75 unsigned long n\_force\_qs\_ngp; 76 #ifdef CONFIG\_RCU\_CPU\_STALL\_DETECTOR 77 unsigned long gp start; 78 unsigned long jiffies\_stall; 79 #endif /\* #ifdef CONFIG\_RCU\_CPU\_STALL\_DETECTOR \*/ 80 long dynticks\_completed; 81 };

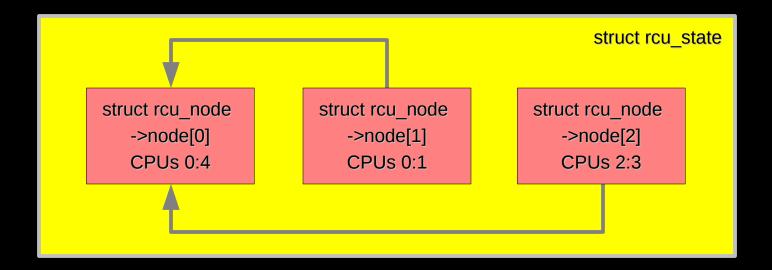


#### **Mapping Data Structures**





#### **Placement of rcu\_node Within rcu\_state**





# **Avoiding Debugging By Process**

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#### **Avoiding Debugging By Process**

# Review your own work carefully See following slides

# Test early, test often, test in small pieces Debugging is 2-3 times harder than writing code Debugging effort rises as the square of the amount of new code added to the testing effort

- Where possible, use existing well-tested code –Even if it is a lot more fun to re-invent the wheel
- I would have scorned this advice as late as the early 1990s, but have since learned it the hard way
- And still sometimes has difficulty following it: -http://paulmck.livejournal.com/14639.html



#### **Review Your Own Code Carefully**

#### Paul E. McKenney's self-review rules for complex code:

- -Write the code long hand in pen on paper
- -Correct bugs as you go
- -Copy onto a clean sheet of paper
- -Repeat until the last two versions are identical

#### What constitutes "not complex"?

- -Sequential code, and
- -You test it line-by-line
  - For example, bash script or single-threaded C-code with gdb)

jeist after "fi'm "do-while" ren-preempt-offline-tasks (struct ren-state \* rsp, statevoid struct rea- node \* (mp) } a vacquire root ren node lærk, migrate tasks, updating Theme pointers... (blocked-tasks) put Them all on current index of root which is (safe, simple) commant which is wrrent - (The one or copy stronght bit of grimm) -> and fix ctat-switch stuff to check lack after acq.



static Void reupreempt\_offline\_tasks (struct reu-state \* rsp, struct vou node x rnp) 3 struct ren mode \* ruproot = ren get\_root(); int is; struct toot kep; ster int (rnp== rnproct)reten; if for (2=0; 2< 52; 2++) { 2 2p= # (list-empty(Grnp-> blocked-tasks[i])) { (entimue; tp = list Quitry (

rea-precippt-offline-tarks (struct reastate \* rsp. static void struct reu. node xrnp) 3 int 25 struct list-head \*lp; struct list-head \*lp/voot; struct ran-node \*rnp-root = ran-get-root(rsp); struct task-struct \*tp; if (rup == rup-root) for (i=0; 2<2; 2+7) & (lp-root = lp = 2rnp->blacked-tosts [2]; (lp-root = annp-root - roblexted-tosts[] while (1 list\_lmpty(lp)) & annp-root - roblexted-tosts[] tp= lit-entry(lp->next, type((xtp)); Spin lock (8 rup-root ( lock); in irgs disabled \*/ list-del (& tp -> rece-vorde entry); list-add (& tp -> ren wale entry, lp-root); tp->ren-bioched-made = rup-root; pin-unlock (& rup-root->lock); /\* irgs disabled\*, 3 3

static void rea-precupt-offline-tasks (struct real-state +rsp. strict receivede +rnp) 3 int /list-head \* 1 p; struct struct list head + 1 p-root; rea-mode \* rup-root = rea-get-root (rsp); Struct struct Task-struct + tps if (rnp==rnp-root) return; for (i=0; 222; 2++) { lp= & rnp->blocked\_tasks[2]; lp-root = & rup-root -> blocked-tasks Ei]; while (!list\_empty(lp)) { tp = list\_entry (lp->next, typeif (\*tp), ren\_node\_entry Spin-lock (& rup-root -> lock); 1+ irgs disabled \*1 list-old (Etp -> rai-node-entry); list-add (8+p->ru-node-entry, ep-root); tp => reu-blocked-work= rnp-root; spin-unlock (&rup-root -> lock); /\* irgs disabled \*/ 3 3

3



So, How Well Did I Do?

```
1 static void rcu_preempt_offline_tasks(struct rcu_state *rsp,
                 struct rcu_node *rnp,
 2
 3
                 struct rcu_data *rdp)
 4 {
     int i;
 5
 6
     struct list head *lp;
     struct list_head *lp_root;
 7
 8
     struct rcu_node *rnp_root = rcu_get_root(rsp);
     struct task_struct *tp;
 9
10
11
     if (rnp == rnp_root) {
12
       WARN ONCE(1, "Last CPU thought to be offlined?");
13
       return;
14
     }
     WARN_ON_ONCE(rnp != rdp->mynode &&
15
16
17
            (!list_empty(&rnp->blocked_tasks[0]) |
             !list_empty(&rnp->blocked_tasks[1])));
18
     for (i = 0; i < 2; i++) {
19
       lp = &rnp->blocked tasks[i];
20
       lp_root = &rnp_root->blocked_tasks[i];
       while (!list_empty(lp)) {
21
         tp = list_entry(lp->next, typeof(*tp), rcu_node_entry);
22
23
         spin_lock(&rnp_root->lock); /* irqs already disabled */
24
         list_del(&tp->rcu_node_entry);
25
26
         tp->rcu_blocked_node = rnp_root;
         list_add(&tp->rcu_node_entry, lp_root);
27
         spin_unlock(&rnp_root->lock); /* irgs remain disabled */
28
       }
29
     }
30 }
```

```
1 static int rcu preempt offline tasks(struct rcu state *rsp,
                                         struct rcu node *rnp,
 2
                                         struct rcu_data *rdp)
 3
 4 {
     int i:
 5
 6
     struct list head *lp;
     struct list_head *lp_root;
 7
     int retval;
 9
     struct rcu_node *rnp_root = rcu_get_root(rsp);
     struct task struct *tp;
10
11
12
     if (rnp == rnp root) {
       WARN_ONCE(1, "Last CPU thought to be offlined?");
13
       return 0; /* Shouldn't happen: at least one CPU online. */
14
     }
15
     WARN ON ONCE(rnp != rdp->mynode &&
16
            (!list_empty(&rnp->blocked_tasks[0]) ||
17
             !list_empty(&rnp->blocked_tasks[1])));
18
19
     retval = rcu preempted readers(rnp);
20
     for (i = 0; i < 2; i++) {
21
       lp = &rnp->blocked_tasks[i];
       lp_root = &rnp_root->blocked_tasks[i];
22
23
       while (!list_empty(lp)) {
         tp = list_entry(lp->next, typeof(*tp), rcu_node_entry);
24
         spin lock(&rnp root->lock); /* irgs already disabled */
25
         list_del(&tp->rcu_node_entry);
26
         tp->rcu_blocked_node = rnp_root;
27
         list_add(&tp->rcu_node_entry, lp_root);
28
29
         spin_unlock(&rnp_root->lock); /* irgs remain disabled */
30
       }
31
32
     return retval;
33 }
```



# **Avoiding Debugging By Mechanical Proofs**

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# **Avoiding Debugging By Mechanical Proofs**

 Works well for small, self-contained algorithms -http://lwn.net/Articles/243851/ (QRCU) -http://lwn.net/Articles/279077/ (RCU dynticks I/F) -git://lttng.org/userspace-rcu formal-model (URCU)

However, the need for formal proof often indicates an overly complex design!!!

–Preemptible RCU's dynticks interface being an extreme case in point (http://lwn.net/Articles/279077/)



# **Avoiding Debugging By Statistical Analysis**



# **Avoiding Debugging By Statistical Analysis**

- Different kernel configuration options select different code
- Suppose that more failure occur with CONFIG\_FOO=y –Focus inspection on code under #ifdef CONFIG\_FOO
- But what exactly does "more failures" mean?



## **Avoiding Debugging By Statistical Analysis**

- Different kernel configuration options select different code
- Suppose that more failure occur with CONFIG\_FOO=y –Focus inspection on code under #ifdef CONFIG\_FOO
- But what exactly does "more failures" mean?
  - -That is where the statistical analysis comes in
  - -The "more failures" must be enough more to be statistically significant
  - -One of the most useful classes I took as an undergraduate was a statistics course!



# **Coping With Schedule Pressure**



# **Coping With Schedule Pressure**

- When you are fixing a critical bug, speed counts
- The difference is level of risk
  - The code is *already* broken, so less benefit to using extremely dainty process steps
  - -But only if you follow up with careful process
  - -Which I repeatedly learn the hard way: http://paulmck.livejournal.com/14639.html
  - -Failure to invest a few days in early 2009 cost me more than a month in late 2009!!!
- Long-term perspective required
  - And that means you leave the "blame it on management" game to Dilbert cartoons
  - -Align with management initiatives, for example, "agile development"



# But I Did All This And There Are Still Bugs!!!



## But I Did All This And There Are Still Bugs!!!

- "Be Careful!!! It Is A Real World Out There!!!"
- The purpose of careful software-development practices is to reduce risk
  - -Strive for perfection, but understand that this goal is rarely reached in this world



### But I Did All This And There Are Still Bugs!!!

- "Be Careful!!! It Is A Real World Out There!!!"
- The purpose of careful software-development practices is to reduce risk
  - -Strive for perfection, but understand that this goal is rarely reached in this world

## But you still need to fix your bugs!!!



## The first challenge is locating the bugs



#### The first challenge is locating the bugs —The computer knows where the bugs are



# The first challenge is locating the bugs The computer knows where the bugs are So your job is to make it tell you!

Ways to make the computer tell you where the bugs are:



The first challenge is locating the bugs

- -The computer knows where the bugs are
- -So your job is to make it tell you!

#### •Ways to make the computer tell you where the bugs are:

- -Debugging printk()s and assertions
- -Event tracing and ftrace
- -Lock dependency checker (CONFIG\_PROVE\_LOCKING and CONFIG\_PROVE\_RCU)
- -Static analysis (and pay attention to compiler warnings!!!)
- -Structured testing: Use an experimental approach

-Record all test results, including environment



## The first challenge is locating the bugs

- -The computer knows where the bugs are
- -So your job is to make it tell you!
- -But getting another person's viewpoint can be helpful
  - To 10,000 *educated and experienced* eyes, all bugs are shallow

## Gaining other people's viewpoints



## The first challenge is locating the bugs

- -The computer knows where the bugs are
- -So your job is to make it tell you!
- -But getting another person's viewpoint can be helpful
  - To 10,000 educated and experienced eyes, all bugs are shallow

## Gaining other people's viewpoints

- -Have other people review your code
- -Explain your code to someone else
- -Special case of explaining code: Document it
  - Think of questions you might ask if someone else showed you the code
  - Focus on the parts of the code you are most proud of: Most likely buggy!
  - Try making a copy of the code, removing the comments, and then documenting it: Perhaps the comments are confusing you



## **But What If The Computer Knows Too Much?**

Event tracing for RCU: 35MB of trace events for failure
Way too much to read and analyze by hand
What to do?



## **But What If The Computer Knows Too Much?**

- Event tracing for RCU: 35MB of trace events for each failure
- Way too much to read and analyze by hand all the time
- What to do? Scripting!!!
- How to generate useful scripts:
  - -Do it by hand the first few times
  - -But keep detailed notes on what you did and what you found
  - -Incrementally construct scripts to carry out the most laborious tasks
  - -Eventually, you will have a script that analyzes the failures

But suppose you are working on many different projects?



## **But What If The Computer Knows Too Much?**

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  - -Incrementally construct scripts to carry out the most laborious tasks
  - -Eventually, you will have a script that analyzes the failures
- But suppose you are working on many different projects?
  - -Script the common cases that occur in many projects
  - -Take advantage of tools others have constructed



# **Summary and Conclusions**



## **Summary and Conclusions**

- Avoid Debugging By Design
- Avoid Debugging By Process
- Avoid Debugging By Mechanical Proofs
- Avoid Debugging By Statistical Analysis
- Avoid Schedule Pressure via Long-Term View
- But Even If You Do All This, You Will Still Do Some Debugging (http://lwn.net/Articles/453002/)
  - -Yes, you are living in the real world!!!
  - -Might be painful sometimes, but it sure beats all known alternatives...



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